Analysis and verification on side effect of anti-backlash delay in phase-frequency detector

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Abstract — **The side effect of the anti-backlash delay in digital phase-frequency detector is analyzed. It is shown that the frequency tracking ability of the detector is decreased by the delay, so that the lock-in transition time will increase. Furthermore, it is shown that the side effect is mainly caused by the delay to the front edge of the reset pulse. Both computer simulation and experimental verification shows the analysis is correct. The work gives an insight view of the detector's working principle and will be useful for its designing.**

I. INTRODUCTION

The digital phase-frequency detector (PFD) is often used in modern phase-locked-loop because it could guide the VCO frequency moving in correct direction during the lock-in transition. In the locked-state the ideal PFD should generate very short correction pulse whose width will equal to the edge distance of the two incoming signal. However, the logic circuits, especially the charge pump, could not react unlimited fast, the width of the correction pulse from the unimproved detector will be produced in a non-linear manner to the edge distance if it is very short. The longest edge distance having this non-linearity is called backlash [1] (may also be called dead zone in some literature). Because of the backlash, the output signal spectrum will be corrupted. One excellent method to solve this problem is to introduce a so-called anti-backlash delay [2] and it is used in many PLL integrated circuits. However, no complete discussion is found on the side effects of this delay. In this paper this topic is addressed which will be useful for the designing of the detector.

For the purpose of self-consistence and setting the starting point of the discussion, the paper will first give a brief introduction to the ideal PFD. Next, the function of the anti-backlash delay is introduced and its side effect is also analyzed. Then, the computer simulation result is presented to verify the analysis. Finally, the experimental measured data is compared with the simulation data to show that the simulation is correct.

II. IDEAL PFD

One implementation of the PFD is shown in Fig.1 [3] (an additional delay block has been added for introducing of the anti-backlash delay). The two outputs of the detector could be connected to two charge pumps whose outputs will be combined and sent to loop filter. The function of the circuit could be briefly described as follows:

1) After the reset (trigged by point C being pulled down) the points U and D will always be high.

2) If R has a down transition (R↓) before V↓ after the reset, U will change to low after R↓. Otherwise, D will change to low if V↓ comes first.

3) After U is pulled to low by R↓, it will stay at low until V↓ comes, which will produce the reset that will bring U high again. Similarly, if V↓ comes first after the reset, D will stay low until R↓ comes and trigs the reset.

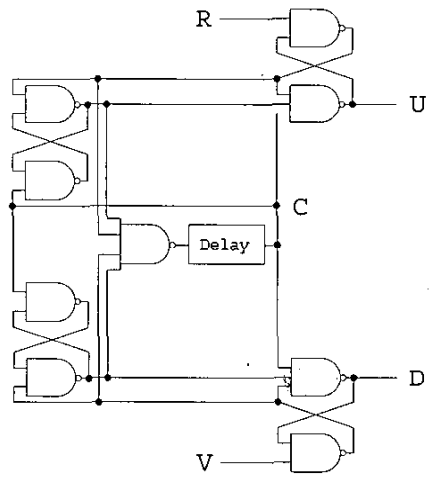

Fig.1 An implementation of PFD. The delay block is for introducing of the anti-backlash delay and its delay time in idcal detector should be zero.

The above function could be shown more clearly by the state graph in Fig.2. Note that since the up transition of R and V will not change the state of U and D, these transitions is not shown in the figure.

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From the state graph the function of the PFD could be intuited easily. Assume the frequency of R is higher than V and the look-in transition is just started, the state changing will be random. So V↓ will randomly bring the detector into both middle and right state. However, once V↓ has brought the detector into the middle state, then the next down transition must be R↓ due to the higher frequency of R. Thus the detector will go to left state and stays there until next V↓ to bring it into middle state again. So after this the detector will just cycle between the middle and left states and never goes to right state anymore. Only U will be pulled low sometime during the cycle. Similarly, if the frequency of R is lower than V the detector will quickly enter the cycle between the middle and right states and only D will be pulled low. Thus the output from the detector will indicate the direction of the frequency error.

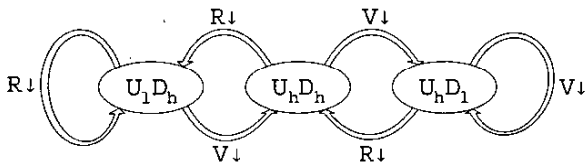

Fig.2 The state graph of the ideal PFD. The superscript h and l indicate the output U or D to be high or low, ↓ indicate high-to-low transition.

Then assume the frequency of R and V are the same with a specific phase difference, and then if R↓ comes before V↓ after the reset, the state evolution will be from middle to left and then from left back to middle. Thus for every cycle U will be pulled low for a time which is proportional to the phase difference of the two signals. If the phase difference is reversed, that is, V↓ comes before R↓ after reset, the state evolution will be from middle to right and then from right back to middle. Thus the output from the detector will indicate both the direction and the magnitude of the phase error.

When the loop is completely locked, the phase error will be very small and the down transition of two input signals will come almost at the same time, and the detector will stay in left or right state only for very short time which causes the output of the detector to be very short pulses. As mentioned in the introduction paragraph, this is the cause of the backlash problem.

III. THE PFD WITH ANTI-BACKLASH DELAY

The anti-backlash delay is introduced to make the circuit of the detector need not to generate very short pulses in the locked state. (This refers to the internal circuit of the detector including the charge pumps. The total output of the detector, on the contrary, will be able to generate very short pulses precisely.) The position to introduce the delay is shown in Fig.1. Specifically, the delay block will introduce delays to both down and up edges of the reset pulse; however, the two delays are not necessary to be equal on length [1].

In the following analysis, the duty cycle of both R and V signal is assumed to be neither very large nor very small. This is to ensure that the up transition of the R and V is separated to their down transition by a time much large than the anti-backlash delay, so that still does not need to be considered in the analysis.

Assume the loop is locked and R↓ comes first after the reset followed very closely by V↓. V↓ will bring D low, however, point C will not be pulled low until the delay time to the down edge is passed. So that instead of only U becoming low for a very short time equals to the edge difference of R and V, both U and D will be low for the time that is at least equal to the anti-backlash delay time and the time difference between U and D staying low will equal to the edge difference. Since the output current from up and down charge pumps will cancel each other if both U and D become low, the detector will still give an output same as that of ideal detector. But now both U and D contain the same dynamic process (up phase, setting phase, down phase), so that their non-linearity reaction time will be canceled each other and the output from the practical detector will be able to indicate the phase difference very precisely.

The side effect of this approach happens during the lock-in transition of the loop. As mention in the previous section, if the frequency of R is higher than V, the state of the detector will evolve in the cycle of from middle to left and then back to middle. Since the loop is not locked yet, it is possible that R↓ will come very quickly after V↓ generates the reset signal (note that if the loop is locked no down transition will come very quickly after the reset). However, since point C will not be pulled low until the delay time to the down edge of the reset signal is passed, so if R↓ comes before C is pulled low it will have no effect on the state evolution. Another R↓ is needed to bring the detector from middle state to the left state, but very probably, another V↓ will come before R↓ and brings the detector into right state. Thus the detector will evolve in the cycle between the middle and right states, which will output a wrong direction indication for the frequency error. This wrong cycle can only be terminated by two R↓ coming in succession (without a V↓ in between) so that the state could evolve from middle to left again. If the frequency difference of the two signals is small, this wrong cycle could sustain for a quite long time so that the lock-in transition time could be significantly extended.

If R↓ comes after C is pulled low but before C is released high again (due to the delay for the up edge of the

reset signal) its effect on the state evolution will be maintained, but U will not become low until C is released. So that the detector will evolve in the correct cycle but the output strength will be reduced for this cycle. This will also extend the lock-in transition time, but should not as significant as that caused by the down edge delay.

IV. Computer Simulation Result

It will be difficult to analytically estimate the effect of the anti-backlash delay, so a computer simulation is performed. The simulation result is shown in Fig. 3 in which the VCO input voltage is plotted against the transition time. PFD working frequency is set to 212 MHz. The simulation is performed for 3 cases. First the ideal locking transition is simulated, that is, the PFD is assumed to be perfect with no anti-backlash delay. Then, the simulation is performed with the up-edge delay of the reset pulse setting to 1 ns and no down-edge delay. Finally, both the up-edge and down-edge delay are set to 1 ns. The simulation clearly shows that the lock-in transition time is extended and the up-edge delay is the major cause of the effect.

V. Experimental Verification

The simulation is also verified by measurement to one Infineon PMB 2251 transmitter PLL chip. The measured result is shown in Fig. 4. Fig. 5 is the simulation result for the similar boundary condition (due to the lack of data, the down-edge delay for the reset pulse is assumed to be zero). The fitting between the experimental and simulation results is much improved by including the side effect of anti-backlash delay.

VI. Conclusion

It is shown that the side effect of the anti-backlash delay will cause the PFD to output wrong signal for the frequency error, so that the lock-in transition time increased. If the working frequency of the detector is high that the anti-backlash delay becomes comparable to the signal cycle time, the frequency tracking ability will be lost completely. It is also shown that the lock-in transition time is extended mainly by the delay to the up-edge of the reset pulse which is inherent to the approach. In general, the anti-backlash delay improves the output spectrum performance of the PFD toward that of the NOR gate phase detector, but also lowers the frequency tracking ability of the PFD (note the NOR gate phase detector has no frequency tracking ability at all).

References

[1] United Kingdom Patent GB 2345210.

[2] United States Patent 4322643.

[3] Floyd M. Gardner, Phaselock Techniques, 2d ed., John Wiley & Sons, New York, 1979.

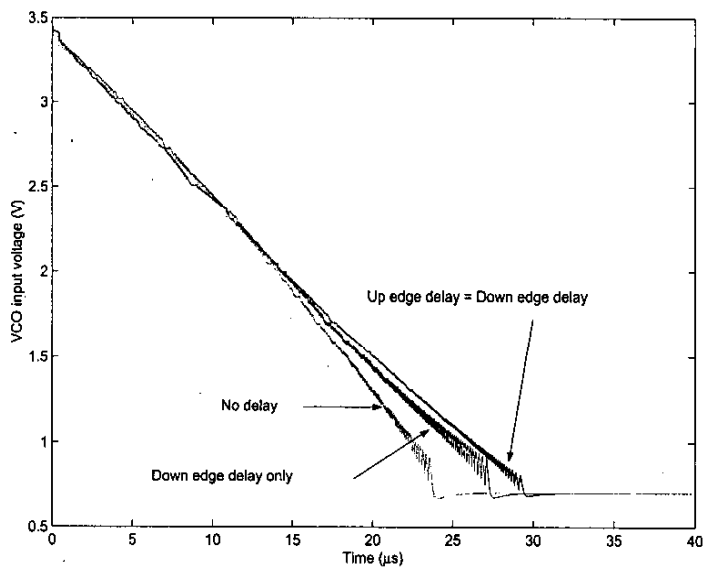

Fig. 3 The computer simulated result for the locking transition with different delay setting.

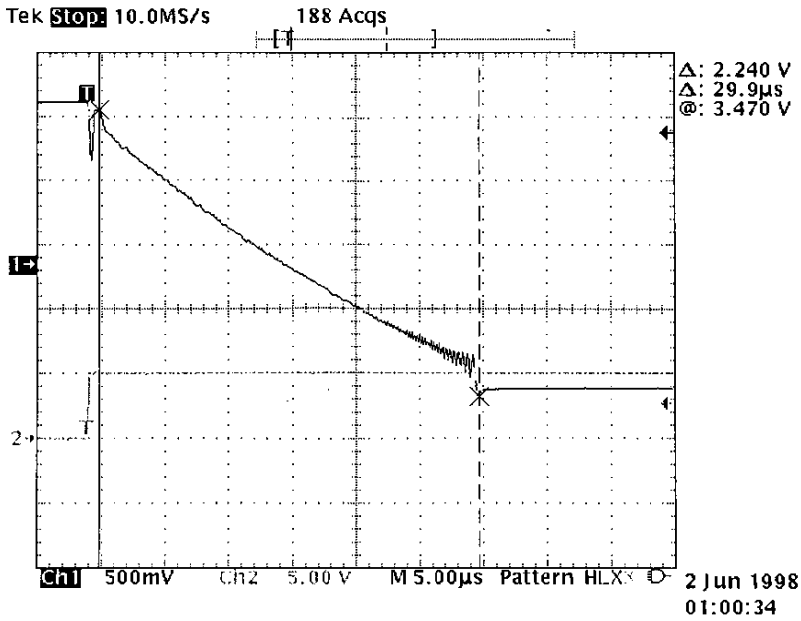

Fig. 4 The measured VCO input voltage during lock-in transition for 890 MHz channel. The working frequency of the PFD is 150 MHz.

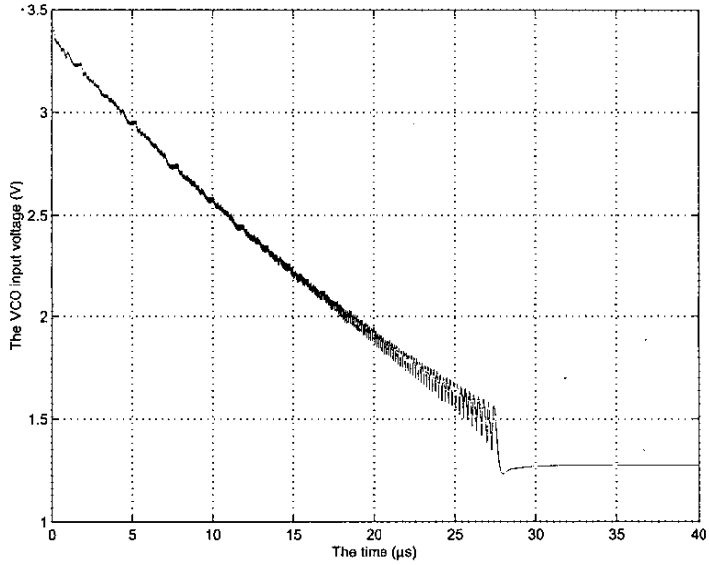

Fig. 5 The simulated lock-in transition with the similar boundary condition used in Fig. 4.